



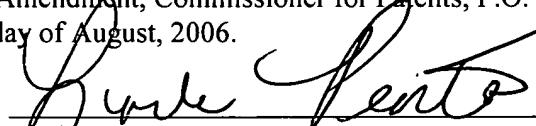
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PATENT
Attorney Docket No. ASC-049C1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S):	Fitzgerald	CONFIRMATION NO.	
SERIAL NO.:	10/774,890	GROUP NO.:	2818
FILING DATE:	February 9, 2004	EXAMINER:	Tran, Mai Huong C.
TITLE:	RELAXED SIGE PLATFORM FOR HIGH SPEED CMOS ELECTRONICS AND HIGH SPEED ANALOG CIRCUITS		

CERTIFICATE OF FIRST CLASS MAILING UNDER 37 C.F.R. 1.8

I hereby certify that this correspondence, and any document(s) referred to as enclosed herein, is/are being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 17th day of August, 2006.


Linda M. Penta

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith is/are:

1. Transmittal Form (1 page);
2. Second Supplemental information Disclosure Statement (2 pgs.);
3. Form USPTO-1449 (1 pg.);
4. Copies of cited references C166-C173); and
5. Return receipt postcard.

<p>TRANSMITTAL FORM</p>	Application Serial Number	10/774,890
	Filing Date	February 9, 2004
	First Named Inventor	Fitzgerald
	Group Art Unit	2818
	Examiner Name	Fitzgerald
	Attorney Docket No.	ASC-049C1
	Patent No.	Not applicable
	Issue Date	Not applicable

ENCLOSURES (check all that apply)

<input type="checkbox"/> Fee Transmittal Form <ul style="list-style-type: none"> <input type="checkbox"/> Check Attached <input type="checkbox"/> Copy of Fee Transmittal Form 	<input type="checkbox"/> Copy of Notice to File Missing Parts of Application	<input type="checkbox"/> Notice of Appeal to Board of Patent Appeals and Interferences
<input checked="" type="checkbox"/> Amendment/Response <ul style="list-style-type: none"> <input type="checkbox"/> Preliminary <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Letter to Official Draftsperson including Drawings [Total Sheets ____] 	<input type="checkbox"/> Formal Drawing(s)	<input type="checkbox"/> Appeal Brief (in triplicate)
	<input type="checkbox"/> Request For Continued Examination (RCE) Transmittal	<input type="checkbox"/> Status Inquiry
	<input type="checkbox"/> Power of Attorney (Revocation of Prior Powers)	<input type="checkbox"/> Return Receipt Postcard
	<input type="checkbox"/> Terminal Disclaimer	<input checked="" type="checkbox"/> Certificate of First Class Mailing under 37 C.F.R. 1.8
<input type="checkbox"/> Petition for Extension of Time	<input type="checkbox"/> Executed Declaration and Power of Attorney for Utility or Design Patent Application	<input type="checkbox"/> Certificate of Facsimile Transmission under 37 C.F.R. 1.8
<input checked="" type="checkbox"/> Supplemental Information Disclosure Statement <ul style="list-style-type: none"> <input checked="" type="checkbox"/> Form PTO-1449 <input checked="" type="checkbox"/> Copies of SIDS Citations (C166-173) 	<input type="checkbox"/> Small Entity Statement	<input type="checkbox"/> Additional Enclosure(s) (please identify below)
<input type="checkbox"/> Certified Copy of Priority Document(s)	<input type="checkbox"/> CD(s) for large table or computer program	
<input type="checkbox"/> Sequence Listing submission <ul style="list-style-type: none"> <input type="checkbox"/> Paper Copy/CD <input type="checkbox"/> Computer Readable Copy <input type="checkbox"/> Statement verifying identity of above 	<input type="checkbox"/> Amendment After Allowance	
	<input type="checkbox"/> Request for Certificate of Correction <ul style="list-style-type: none"> <input type="checkbox"/> Certificate of Correction (in duplicate) 	

CORRESPONDENCE ADDRESS

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 Boston, MA 02109
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SIGNATURE BLOCK

Respectfully submitted,

Natasha C. Us
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PATENT
Attorney Docket No. ASC-049C1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S): Fitzgerald

SERIAL NO.: 10/774,890 GROUP NO.: 2818

FILING DATE: February 9, 2004 EXAMINER: TRAN, MAI HUONG C.

TITLE: RELAXED SIGE PLATFORM FOR HIGH SPEED CMOS
ELECTRONICS AND HIGH SPEED ANALOG CIRCUITS

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with the provisions of 37 C.F.R. 1.97 and 1.98, Applicants hereby make of record the publications listed on the accompanying Form PTO-1449, and other information contained herein, for consideration by the Examiner in connection with the examination of the above-identified patent application. In accordance with 37 C.F.R. 1.98(a)(2), only copies of the non-patent publications are enclosed.

REMARKS

In accordance with the provisions of 37 C.F.R. 1.97, this statement is being filed (CHECK ONE):

(1) within three (3) months of the filing date of a national application other than a continued prosecution application under 37 C.F.R. 1.53(d), or within three (3) months of the date of entry of the national stage as set forth in 37 C.F.R. 1.491 in an international application, or before the mailing of the first Office action on the merits, or before the mailing of a first Office action after the filing of a request for continued examination under 37 C.F.R. 1.114; or

(2) after the period defined in (1) but before the mailing date of a final action or a notice of allowance under 37 C.F.R. 1.311, and

the requisite Statement is below, OR

the requisite fee under 37 C.F.R. 1.17(p), namely \$180.00, is included herein, or

(3) after the mailing date of a **final action or notice of allowance** but before the payment of the **issue fee**, AND

the requisite Statement is below, AND

the requisite petition fee under 37 C.F.R. 1.17(p), namely **\$180.00** is included herein.

It is respectfully requested that each of the publications listed on the attached Form PTO-1449, and other information contained herein, be made of record in this application.

STATEMENT

As required under 37 C.F.R. 1.97(e), Applicant(s), through the undersigned, hereby state either that [check the appropriate space only if either (2) or (3) is checked on the previous page and the Statement is required]:

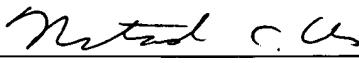
1. Each item of information contained in the Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application **not more than three months** prior to the filing of the Information Disclosure Statement; or

2. No item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing this Statement after making reasonable inquiry, no item of information contained in the Information Disclosure Statement was known to **any individual** designated in 37 C.F.R. 1.56(c) **more than three months** prior to the filing of the Information Disclosure Statement.

Respectfully submitted,

Date: August 17, 2006
Reg. No. 44,381

Tel. No.: (617) 570-1806
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FORM PTO - 1449

SECOND SUPPLEMENTAL INFORMATION
DISCLOSURE STATEMENT

ATTY DOCKET NO.: ASC-049C1

APPLICANT: Fitzgerald
 SERIAL NO.: 10/774,890
 FILING DATE: February 9, 2004
 EXAMINER: Tran, Mai Huong C.
 GROUP: 2818

U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE

OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
	C166	Kubota M., et al. "New SOI CMOS Process with Selective Oxidation," IEEE IEDM TECH. DIG., pp. 814-816, (1986).
	C167	Ming et al., "Interfacial roughness scaling and strain in lattice mismatched Si _{0.4} Ge _{0.6} thin films on Si" Applied Physics Letters, Vol. 67, No. 5, July 31, 1995, pp. 629-631.
	C168	Ming et al., "Microscopic structure of interfaces in Si _{1-x} Ge _x /Si heterostructures and superlattices studied by x-ray scattering and fluorescence yield," Physical Review B, Vol. 47, No. 24, pp. 373-81, June 15, 1993.
	C169	Nishi et al. "Handbook of Semiconductor Manufacturing Technology," Marcel Dekker AG, New York, NY, 2000, pp. 1-22
	C170	O'Neill, et al., "Deep Submicron CMOS Based on Silicon Germanium Technology," Fellow, IEEE Transactions on Electron Devices, Vol. 43, No. 6, June 1996 pp. 911-918.
	C171	Sugii, et al., "Role of Si _{1-x} Ge _x buffer layer on mobility enhancement in a strained-Si channel metal-oxide-semiconductor field-effect transistor," Central Research Laboratory, Hitachi Ltd. 1-280 Higashi-Koigakubo, Kokubunji-shi, Tokyo 185-8601 Japan, pp. 2948-2950.
	C172	Vossen et al. "Thin Film Processes II" Academic Press Inc., San Diego, CA, 1991, pp. 370-442.
	C173	Wolfe et al. "Silicon Processing for the VLSI Era, Volume 1; Process Technology," Lattice Press 1986, pp. 124-160.

EXAMINER	DATE CONSIDERED